MULTIMEDIA UNIVERSITY

STUDENT ID NO

TABLE NO:

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

TSN1101 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All Sections /Groups)

28 FEBRUARY 2017
2.30 p.m. - 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of **EIGHTEEN pages (excluding this page and the Appendix)** with **TWO SECTIONS.** Each section contains **FOUR** questions.

2. Attempt a total of **FIVE** questions, with a maximum of **THREE** questions from any one SECTION and the remaining **TWO** questions from the other SECTION. Each question carries **12 marks** and the distribution of the marks for each subdivision is given. Maximum allotted marks are **60 marks.**

3. Please **write all your answers in the Question Paper itself** in the space provided.

SECTION A

QUESTION A1:

a. Convert the Binary number 101101_2 into the following number systems:
   i. Decimal
   ii. Octal
   iii. Hexadecimal
   iv. Gray Code

(4 ×1=4 marks)

b. Perform the following binary arithmetic operation:

i. 1101 + 1011
ii. 1010 – 0111

(2 x 1 = 2 marks)

Continued...

c. i. What is an 'Overflow condition' during addition of signed numbers?

ii. When does an 'Overflow condition' occur?

(2 marks)

d. Perform the binary addition using 8 bit **2's complement** form for the following decimal numbers:

i. 33 and 15

ii. - 46 and 25

(2x 2=4 marks)

Continued...

QUESTION A2:

a. Simplify the following expression using Boolean algebra:
$A\bar{B} + A\bar{B}C + A\bar{B}CD + A\bar{B}CDE$

(2 marks)

b. For the Boolean function $F = A + \bar{C}D + AC\bar{D} + \bar{A}BC\bar{D}$:

i. Obtain the truth table for F **(4 marks)**
ii. Use Karnaugh Map (K map) to simplify F. **(3 marks)**
iii. Draw the logic diagram for the simplified function F as in (ii) above. **(3 marks)**

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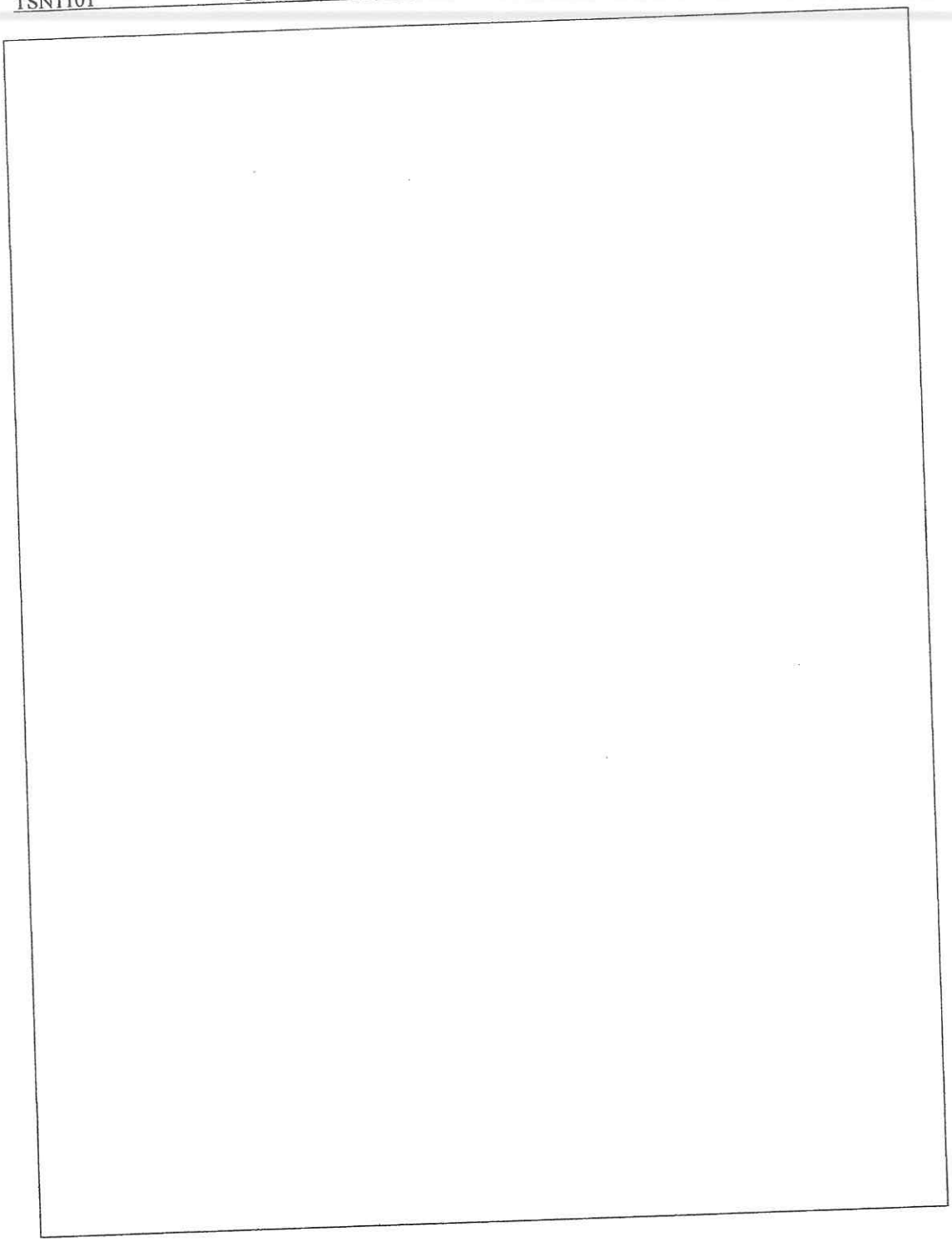

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QUESTION A3:

a. For the input combinations 010, 100, 001, 011, a HIGH output will be presented in decoding. For other input combinations, the outputs are LOW. Implement the circuit for the above with a suitable decoder and necessary logic gates.

i. Write down the truth table **(2 marks)**

ii. Expression for the output function **(1 mark)**

iii. Draw the logic diagram of the implemented decoder **(2 marks)**

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b. Implement the following Boolean function with a suitable multiplexer:

$F(A, B, C, D) = \Sigma m(1,3,4,11,12,13,14,15)$

i. Write down the truth table with the output function **(4 marks)**

ii. Draw the multiplexer implementation **(3 mark)**

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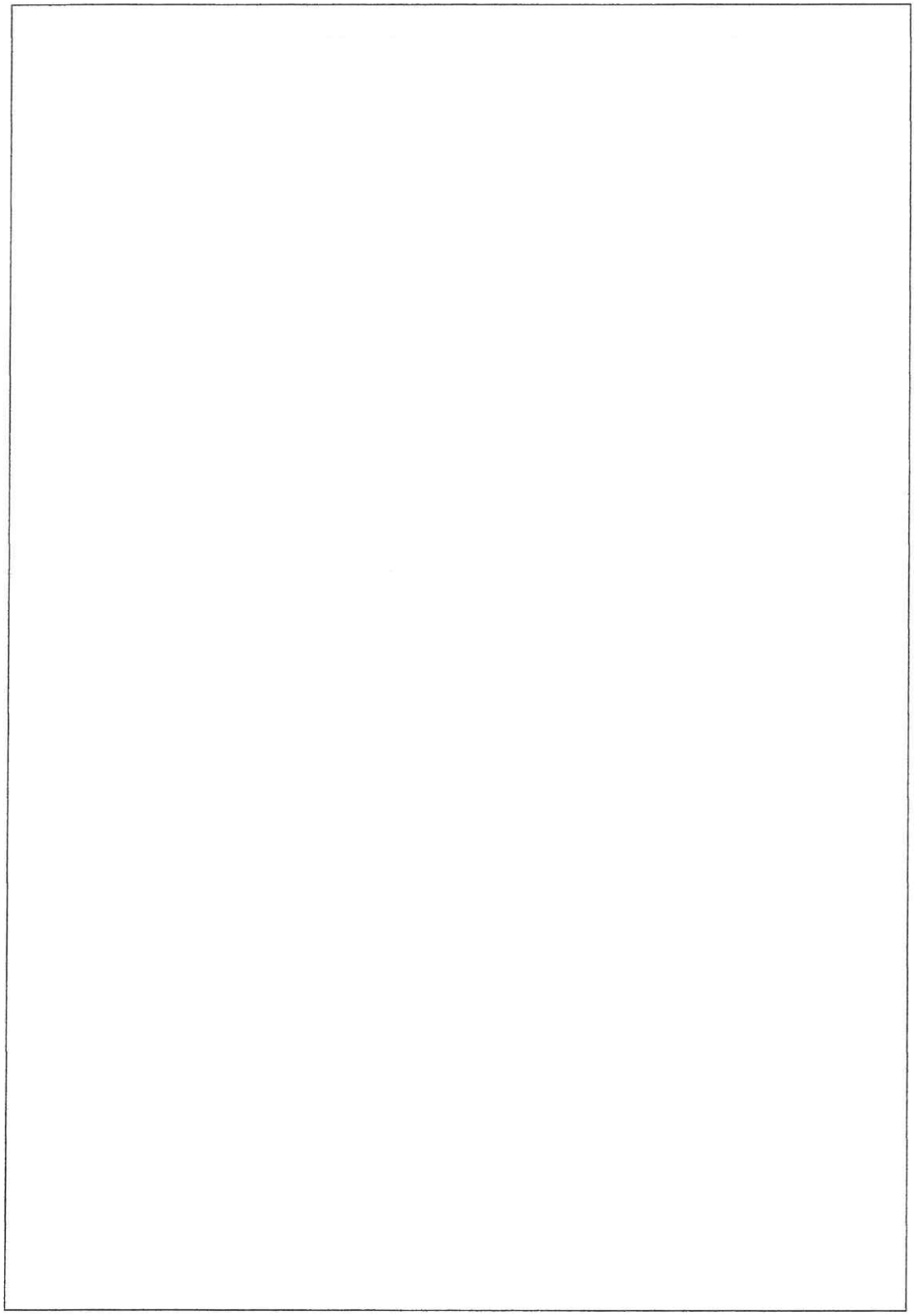

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QUESTION A4:

a. A synchronous counter has two negative-edged triggered D flip-flops and three inputs X, Y and Z. Design the counter based on the two conditions listed below:
   - If Z is 0, X and Y will count up based on the present state of X and Y.
   - If Z is 1, X and Y will count down based on the present state of X and Y.

   i..Complete the excitation table.

   (4 marks)

   ii .Simplify D_X and D_Y using K-maps.

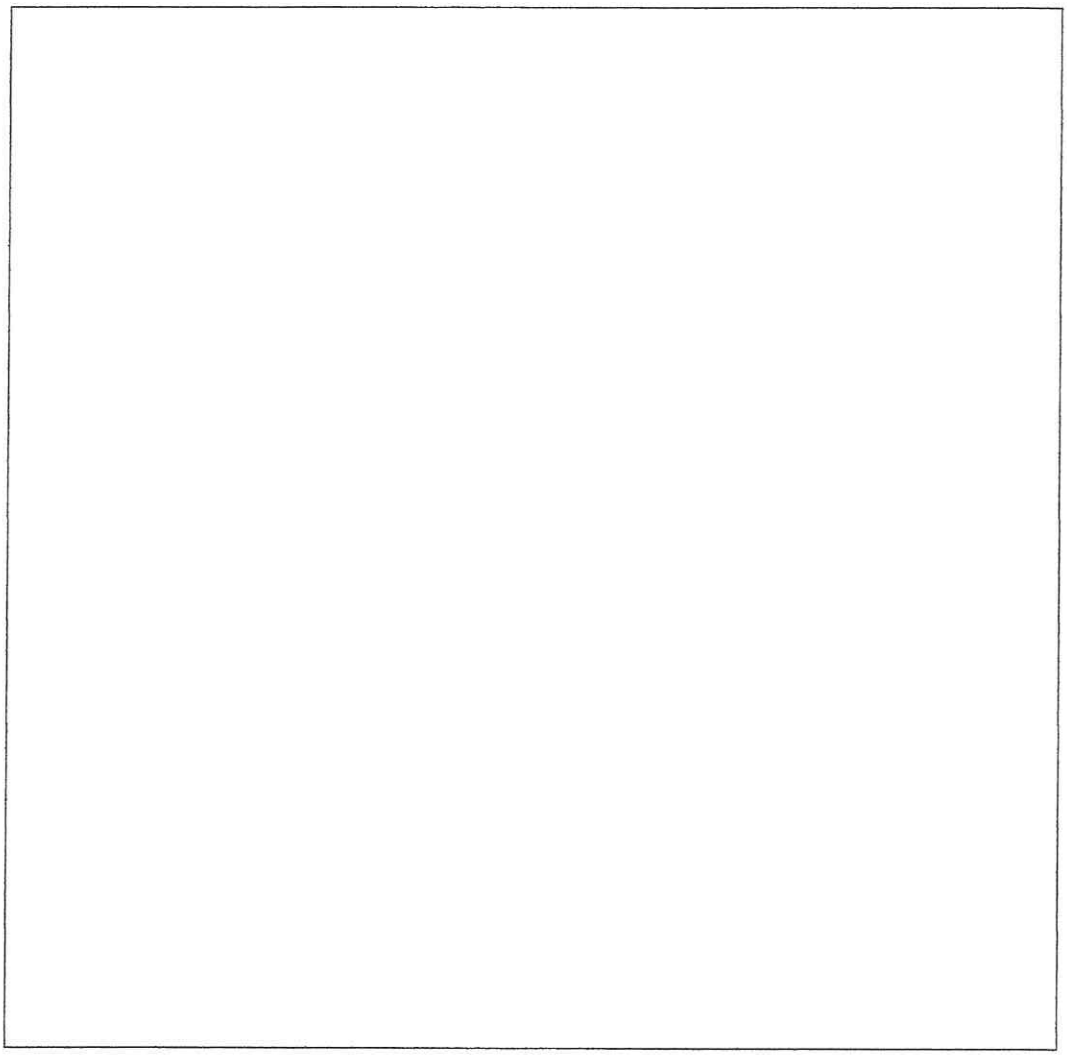
   (2 marks)

   iii .Draw the synchronous counter.

   (3 marks)

Continued...

b. Draw a 2-bit binary ripple DOWN counter using positive-edge triggered JK flip flops.
(2 marks)



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SECTION B

QUESTION B1

a. The processing required for a single instruction is called an instruction cycle. A simplified three step cycle will include the fetch, execute and interrupt cycles. Draw the three step instruction cycle.

(3 marks)

b. The system bus is a communication pathway connecting major computer components such as processor, memory and I/O. The three common buses are the data lines, address lines and control lines. How are these buses used in a computer system?

(3 marks)

Continued...

c. Many processor designs include a register or set of registers, often known as the program status word (PSW), that contain status information. The PSW typically contains condition codes plus other status information. List four common fields or flags of the PSW.

(2 marks)

d. Assume that a processor that employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR). During the fetch cycle, an instruction is read from memory. List the flow of data during this cycle in the correct order.

(4 marks)

Continued...

QUESTION B2

a. Assume a three-stage pipeline (fetch, decode & execute). Draw a timing diagram to show how many units are needed for four instructions.

(3 marks)

b. Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR), supporting only one-address instructions. List the symbolic sequence of micro-operations for an indirect cycle.

(1.5 marks)

Continued...

c. Assume that Word 11 contains 22, Word 22 contains 33, Word 33 contains 44, and Word 44 contains 55. Given the memory values above and a one-address machine with an Accumulator (Register A), what values do the following instructions load into the Accumulator?

i.	LOAD IMMEDIATE 22	ii.	LOAD DIRECT 22
iii.	LOAD INDIRECT 22	iv.	LOAD IMMEDIATE 33
v.	LOAD DIRECT 33	vi.	LOAD INDIRECT 33

(3 marks)

d. In processor pipelines, in order to overcome branch hazards, various branch prediction techniques can be used. These techniques can be either static or dynamic. What are the THREE static branch prediction techniques?

(1.5 marks)

Continued...

e. The Intel 8085 has 5 addressing modes. State any three of the addressing modes and list an instruction from each mode.

(3 marks)

QUESTION B3

a. One of the distinctions among memory types is the method of accessing units of data such as **sequential access, direct access** and **random access.** Explain each of them by giving example.

(3 marks)

Continued...

b. I/O modules vary considerably in complexity and the number of external devices that they control. Draw a general block diagram of an I/O module that consists of data registers, status registers, bus, address and control lines and etc. Illustrate how the I/O module performs its functions in it.

(4 marks)

Continued...

c. The organizational changes in processor design have primarily been focused on increasing instruction-level parallelism, so that more work could be done in each clock cycle. Explain the term of **pipelining, superscalar** and **simultaneous multithreading (SMT)** with respect to parallelism in multi-core computing.

(3 marks)

d. **Snoopy protocols** distribute the responsibility for maintaining **cache coherence** among all of the cache controllers in a multiprocessor. One of the basic approaches to the snoopy protocol is '**write invalidate**'. Explain how '**write invalidate**' is able to maintain cache coherence.

(2 marks)

Continued...

QUESTION B4

a. State any **TWO** types of addressing mode of instructions that involve memory access with examples from 8085.

(2 marks)

b. Given the following register and memory values for an Intel 8085 microprocessor, what values are in the Accumulator (Register A) after these instructions are executed? (Assume that each instruction is not related)

- Register A contains 40H
- Register B contains 70H
- Register C contains 05H
- Register H contains 50H
- Register L contains 01H

Memory addresses:

4050H	10H
5001H	20H
6020H	30H
7005H	40H

i. MVI D, 30H
ii. LDAX B
iii. MOV A, M
iv. MVI A, 30H
v. MOV A, B
vi. MOV M, A
vii. ADD M
viii. ADD C

(4 marks)

Continued...

c. SIX numbers are stored in memory locations from 6001H to 6006H. Write an 8085 ALP to increment the numbers in these memory locations by 2.

(3 marks)

d. Write an 8085 ALP to find the 2's complement of a 16-bit number in locations 5000H and 5001H (lower order first followed by higher order) and store the 16 bit result in 6500H and 6501H.

(3 marks)

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